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L1	1161	716/18	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/09 15:15
L2	1464	716/2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/09 15:11
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L5	215	326/104	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/09 15:12
L6	187	326/10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/09 15:12
L7	1	(716/18).ccls. and (scalable adj (logic adj circuit\$2)) and (variables) and (small\$2 adj depth)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/09 15:21
L8	0	(716/2).ccls. and (scalable adj (logic adj circuit\$2)) and (variables) and (small\$2 adj depth)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/09 15:21
L9	0	(716/3).ccls. and (scalable adj (logic adj circuit\$2)) and (variables) and (small\$2 adj depth)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/09 15:22

L10	0	(716/7).ccls. and (scalable adj (logic adj circuit\$2)) and (variables) and (small\$2 adj depth)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/09 15:22
L11	0	(326/104).ccls. and (scalable adj (logic adj circuit\$2)) and (variables) and (small\$2 adj depth)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/09 15:22
L12	0	(326/10).ccls. and (scalable adj (logic adj circuit\$2)) and (variables) and (small\$2 adj depth)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/09 15:22
L13	1	("716"/\$).ccls. and (scalable adj (logic adj circuit\$2)) and (variables) and (small\$2 adj depth)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/09 15:23
L14	1	(scalable adj (logic adj circuit\$2)) and (variables) and (small\$2 adj depth)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/09 15:24
L15	0	(logic adj circuit\$2) and (gate types) and (top adj portion) and (lower adj portion) and (variables) and (small\$2 adj depth)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/09 15:28
L16	0	(logic adj circuit\$2) and (top adj lower adj portion\$2) same ((two adj input) adj gates) and (depth)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/09 15:30
L17	17	(logic adj circuit\$2) and ((two adj input) adj gates) and (depth)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/09 15:31
L18	2	(logic adj circuit\$2) and ((two adj input) adj gates) and (depth adj between)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/09 15:31

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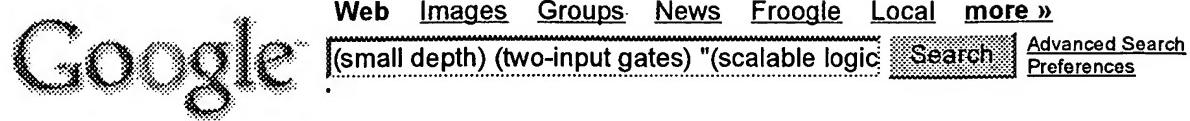
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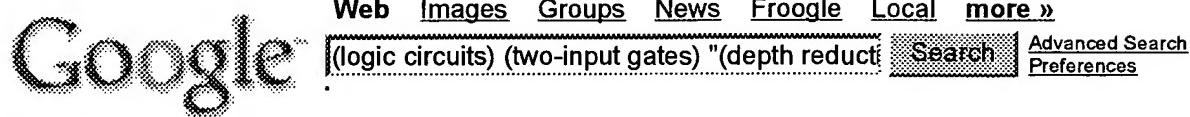
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